

ULTRA-LOW IMPEDANCE POWER  
INTERCONNECTION SYSTEM FOR ELECTRONIC PACKAGES

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application claims benefit of the following provisional patent applications,  
which are hereby incorporated by reference herein.

Application Serial No. 60/266,941, entitled "MECHANICAL  
INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT  
FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by Joseph  
10 T. DiBene II, David H. Hartke, and James M. Broder, filed February 6, 2001;

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL  
MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE  
MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad  
Raiszadeh, filed March 19, 2001;

15 Application Serial No. 60/287,860, entitled "POWER TRANSMISSION  
DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian,  
filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE  
HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION  
20 MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE  
POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E.  
Hoge, and Edward J. Derian, filed May 16, 2001;

Application Serial No. 60/292,125, entitled "VORTEX HEATSINK FOR LOW  
25 PRESSURE DROP HIGH PERFORMANCE THERMAL MANAGEMENT  
ELECTRONIC ASSEMBLY SOLUTIONS," by Joseph T. DiBene II, Farhad Raiszadeh,  
filed May 18, 2001;

Application Serial No. 60/299,573, entitled "IMPROVED MICRO-I-PAK STACK-  
UP ARCHITECTURE," by Joseph T. DiBene, Carl E. Hoge, and David H. Hartke, filed  
30 June 19, 2001;

Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY  
USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A  
MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed  
June 27, 2001;

Patent # 6,369,901

Application Serial No. 60/304,929, entitled "BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001;

Application Serial No. 60/304,930, entitled "MICRO-I-PAK," by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001;

5        Application Serial No. 60/310,038, entitled "TOOL-LESS CONCEPTS FOR BORREGO," by Edward J. Derian and Joseph T. DiBene II, filed August 3, 2001;

Application Serial No. 60/313,338, entitled "TOOL-LESS PRISM IPA ASSEMBLY TO SUPPORT IA64 MCKINLEY MICROPROCESSOR," by David H. Hartke and Edward J. Derian, filed August 17, 2001; and

10       Application Serial No. --/---,---, entitled MICRO-SPRING CONFIGURATIONS FOR POWER DELIVERY FROM VOLTAGE REGULATOR MODULES TO INTEGRATED CIRCUITS AND MICROPROCESSORS, by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed November 8, 2001.

This patent application is also continuation-in-part of the following co-pending and  
15       commonly assigned patent applications, each of which applications are hereby incorporated by reference herein:

Application Serial No. 09/885,780, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed June 19, 2001, which is a continuation in-part of application Serial No. 09/353,428, entitled "INTER-CIRCUIT  
20       ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

Application Serial No. 09/432,878, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY," by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999, which is a continuation-in-part of Application Serial No.  
25       09/353,428, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY" by Joseph T.  
30       DiBene II and David Hartke, filed November 28, 2000, which claims priority to the following U.S. Provisional Patent Applications:

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Application Serial No. 60/167,792, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed November 29, 1999;

Application Serial No. 60/171,065, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed December 16, 1999;

Application Serial No. 60/183,474, entitled "DIRECT ATTACH POWER/THERMAL WITH INCEP," by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGH AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,506, entitled "HIGH PERFORMANCE THERMAL MECHANICAL INTERFACE," by Wendell C. Johnson, David H. Hartke and Joseph T. DiBene II, filed July 20, 2000;

Application Serial No. 60/219,813, entitled "HIGH-CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEAT SINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000; and

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Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II, James J. Hjerpe, , filed September 14, 2000;

5 . Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II, David H. Hartke, James J. Hjerpe Kaskade, and Carl E. Hoge, filed February 16, 2001, which claims priority to the following Provisional Patent Applicaitons;

10 Application Serial No. 60/183,474, entitled "DIRECT ATTACH POWER/THERMAL WITH INCEP," by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

Application Serial No. 60/186,769, entitled "THERMACEP SPRING BEAM," by Joseph T. DiBene II and David H. Hartke, filed March 3, 2000;

15 Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

20 Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGH AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene and David H. Hartke, filed April 10, 2000;

25 Application Serial No. 60/219,506, entitled "HIGH PERFORMANCE THERMAL MECHANICAL INTERFACE," by Wendell C. Johnson, David H. Hartke and Joseph T. DiBene II, filed July 20, 2000;

Application Serial No. 60/219,813, entitled "HIGH-CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

30 Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

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Application Serial No. 60/222,407, entitled "VAPOR HEAT SINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000; and

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II, James J. Hjerpe, , filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by David H. Hartke, James M. Broder, Joseph T. DiBene II, filed February 6, 2001; and

Application Serial No. 09/798,541, entitled "THERMAL/MECHANICAL SPRINGBEAM MECHANISM FOR HEAT TRANSFER FROM HEAT SOURCE TO HEAT DISSIPATING DEVICE," by Joseph T. DiBene II, David H. Hartke, Wendell C. Johnson, and Edward J. Derian, filed March 2, 2001, which is a continuation-in-part of Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed November 28, 2000, and a continuation-in-part of Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II and David H. Hartke, filed February 16, 2001, and a continuation in part of Application Serial No. 09/432,878, entitled "INTER-CIRCUIT

ENCAPSULATED PACKAGING FOR POWER DELIVERY”, by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999, which is a continuation in part of Application Serial No. 09/353,428, entitled “INTER-CIRCUIT ENCAPSULATED PACKAGING,” by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent  
5 No. 6,304,450, and which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/183,474, entitled “DIRECT ATTACH POWER/THERMAL WITH INCEP,” by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

10 Application Serial No. 60/186,769, entitled “THERMACEP SPRING BEAM,” by Joseph T. DiBene II and David H. Hartke, filed March 3, 2000;

Application Serial No. 60/187,777, entitled “NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED  
15 PACKAGING TECHNOLOGY,” by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled “EMI FRAME WITH POWER FEED-THROUGH AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE,” by Joseph T. DiBene and David H.  
20 Hartke, filed April 10, 2000;

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Application Serial No. 60/219,813, entitled “HIGH-CURRENT  
25 MICROPROCESSOR POWER DELIVERY SYSTEMS,” by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled “HIGH DENSITY CIRCULAR ‘PIN’ CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT,” by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

30 Application Serial No. 60/222,407, entitled “VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT,” by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000; and

ENCAPSULATED PACKAGING FOR POWER DELIVERY

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II, James J. Hjerpe, , filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

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Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by David H. Hartke, James M. Broder, Joseph T. DiBene II, filed February 6, 2001; and

Application Serial No. 09/801,437, entitled "METHOD AND APPARATUS FOR DELIVERING POWER TO HIGH PERFORMANCE ELECTRONIC ASSEMBLIES" by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, James M. Broder, Edward J. Derian, Joseph S. Riel, and Jose B. San Andres, filed March 8, 2001, which is a continuation in part of the following patent applications:

Application Serial No. 09/798,541, entitled "THERMAL/MECHANICAL SPRINGBEAM MECHANISM FOR HEAT TRANSFER FROM HEAT SOURCE TO HEAT DISSIPATING DEVICE," by Joseph T. DiBene II, David H. Hartke, Wendell C. Johnson, and Edward J. Derian, filed March 2, 2001;

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Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY" by Joseph T. DiBene II and David Hartke, filed November 28, 2000;

Application Serial No. 09/432,878, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY," by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999, which is a continuation-in-part of Application Serial No. 09/353,428, entitled "INTER-CIRCUIT

ENCAPSULATED PACKAGING, David H. Hartke, filed July 15, 1999 and now issued as and which claims priority to the following Applications:

Application Serial No. 60/18 PACKAGING FOR EMI CONTAINMENT THERMAL DISSIPATION USING ENCAPSULATED PACKAGING TECHNOLOGY," David H. Hartke, filed March 8, 2000;

Application Serial No. 60/18 WITH POWER FEED-THROUGH AND THERMAL DISSIPATION IN AN AGGREGATE DIAMOND MIXTURE, by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled "HIGH-CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

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Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

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Application Serial No. 09/802,329, entitled "METHOD AND APPARATUS FOR THERMAL AND MECHANICAL MANAGEMENT OF A POWER REGULATOR MODULE AND MICROPROCESSOR IN CONTACT WITH A THERMALLY CONDUCTING PLATE" by Joseph T. DiBene II and David H. Hartke, filed March 8, 2001, which is a continuation in part of the following patent applications:

Application Serial No. 09/798,541, entitled "THERMAL/MECHANICAL SPRINGBEAM MECHANISM FOR HEAT TRANSFER FROM HEAT SOURCE TO HEAT DISSIPATING DEVICE," by Joseph T. DiBene II, David H. Hartke, Wendell C. Johnson, and Edward J. Derian, filed March 2, 2001, which is a continuation-in-part of Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed November 28, 2000, and a continuation-in-part of Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II and David H. Hartke, filed February 16, 2001, and a continuation in part of Application Serial No. 09/432,878, entitled

“INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY”, by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999, which is a continuation in part of Application Serial No. 09/353,428, entitled “INTER-CIRCUIT ENCAPSULATED PACKAGING,” by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

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Application Serial No. 60/187,777, entitled “NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY,” by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

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Application Serial No. 09/910,524, entitled "HIGH PERFORMANCE THERMAL/MECHANICAL INTERFACE FOR FIXED-GAP REFERENCES FOR HIGH HEAT FLUX AND POWER SEMICONDUCTOR APPLICATIONS", by Joseph T. DiBene, II, David H. Hartke, Wendell C. Johnson, Farhad Raiszadeh, Edward J. Darien

and Jose B. San Andres, filed July 20, 2001, which is a continuation in part of the following patent applications:

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APPLICATIONS", by Joseph T. DiBene, II, David H. Hartke, Wendell C. Johnson, Farhad Raiszadeh, Edward J. Darien and Jose B. San Andres, filed July 20, 2001;

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Application Serial No. 09/802,329, entitled "METHOD AND APPARATUS FOR THERMAL AND MECHANICAL MANAGEMENT OF A POWER REGULATOR MODULE AND MICROPROCESSOR IN CONTACT WITH A THERMALLY CONDUCTING PLATE" by Joseph T. DiBene II and David H. Hartke, filed March 8, 2001;

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Application Serial No. 09/798,541, entitled "THERMAL/MECHANICAL COUPLING BEAM MECHANISM FOR HEAT TRANSFER FROM HEAT SOURCE TO HEAT DISSIPATING DEVICE," by Joseph T. DiBene II, David H. Hartke, Wendell C. Johnson, and Edward J. Derian, filed March 2, 2001, which is a continuation-in-part of Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed November 10, 2000, and a continuation-in-part of Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II and David H. Hartke, filed February 16,

20

2001, and a continuation in part of Application Serial No. 09/432,878, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY", by Joseph T. DiBene II and David H. Hartke, filed November 2,

1999, which is a continuation in part of Application Serial No. 09/353,428, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

5                   Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II, David H. Hartke, James J. Hjerpe Kaskade, and Carl E. Hoge, filed February 16, 2001;

10                  Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY" by Joseph T. DiBene II and David Hartke, filed November 28, 2000;

15                  Application Serial No. 09/432,878, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY," by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999, which is a continuation-in-part of Application Serial No. 09/353,428, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

and which claims priority to the following U.S. Provisional Patent Applications:

20                  Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

25                  Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGH AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene and David H. Hartke, filed April 10, 2000;

30                  Application Serial No. 60/219,813, entitled "HIGH-CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000; and

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II, James J. Hjerpe, , filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by David H. Hartke, James M. Broder, Joseph T. DiBene II, filed February 6, 2001; and

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Farhad Raiszadeh and Edward J. Derian, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

5           Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 16, 2001;

10           Application Serial No. 60/292,125, entitled "VORTEX HEATSINK FOR LOW PRESSURE DROP HIGH PERFORMANCE THERMAL MANAGEMENT ELECTRONIC ASSEMBLY SOLUTIONS," by Joseph T. DiBene II and Farhad Raiszadeh, filed May 18, 2001;

          Application Serial No. 60/299,573, entitled "MICRO I-PAK STACK UP ARCHITECTURE," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, , filed June 19, 2001;

15           Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke , filed June 27, 2001;

20           Application Serial No. 60/304,929, entitled "BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001;

          Application Serial No. 60/304,930, entitled "MICRO I-PAK," by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, Edward J. Derian, filed July 11, 2001; and

25           Application Serial No. 60/310,038, entitled "TOOL-LESS CONCEPTS FOR BORREGO," by Edward J. Derian and Joseph T. DiBene II, filed August 3, 2001;

30           Application Serial No. 60/313,338, entitled "TOOL-LESS PRISM IPA ASSEMBLY TO SUPPORT IA64 MCKINLEY MICROPROCESSOR," by David H. Hartke and Edward J. Derian, filed August 17, 2001;

          Application Serial No. --/---,---, entitled "MICRO-SPRING CONFIGURATIONS FOR POWER DELIVERY FROM VOLTAGE

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REGULATOR MODULES TO INTEGRATED CIRCUITS AND MICROPROCESSORS,” by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed November 8, 2001.

5

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to systems and methods for interconnecting electronic packages and in particular to a power interconnection system mating between substrates to enable a low impedance disconnectable power delivery path between the power source and the load of an electronic package.

10

2. Description of the Related Art

High-speed microprocessor packaging must be designed to provide increasingly small form-factors. Meeting end user performance requirements with minimal form-factors while increasing reliability and manufacturability presents significant challenges in the areas of power distribution, thermal management, and electromagnetic interference (EMI) containment.

15

To increase reliability and reduce thermal dissipation requirements, newer generation processors are designed to operate with reduced voltage and higher current. Unfortunately, this creates a number of design problems.

20

First, the lowered operating voltage of the processor places greater demands on the power regulating circuitry and the conductive paths providing power to the processor. Typically, processors require supply voltage regulation to within 10% of nominal. In order to account for impedance variations in the path from the power supply to the processor itself, this places greater demands on the power regulating circuitry, which must then typically regulate power supply voltages to within 5% of nominal.

25

Lower operating voltages have also lead engineers away from centralized power supply designs to distributed power supply architectures in which power is bused where required at high voltages and low current, where it is converted to the low-voltage, high-current power required by the processor from nearby power conditioning circuitry.

30

While it is possible to place power conditioning circuitry on the processor package itself, this design is difficult to implement because of the unmanageable physical size of the

components in the power conditioning circuitry (e.g. capacitors and inductors), and because the addition of such components can have a deleterious effect on processor reliability. Such designs also place additional demands on the assembly and testing of the processor packages as well.

5 Further exacerbating the problem are the transient currents that result from varying demands on the processor itself. Processor computing demands vary widely over time, and higher clock speeds and power conservation techniques such as clock gating and sleep mode operation give rise to transient currents in the power supply. Such power fluctuations can require changes of thousands of amps within a few microseconds. The resulting current  
10 surge between the processor and the power regulation circuitry can create unacceptable spikes in the power supply voltage (e.g.  $dv = IR + L \frac{di}{dt}$ ).

The package on which the device (die) typically resides must be connected to other circuitry in order for it to communicate and get power into and out of the device. Because the current slew-rates may be very high, a low impedance interconnection system is often  
15 needed to reduce voltage excursions between the power source and load which, if left unchecked, may cause false switching due to the reduced voltage seen at the load from a large voltage drop across the interconnect.

The technology of vertically stacking electronic substrates has been utilized for a number of years. As one example, U.S. Patent No. 5,734,555, issued to McMahon (which is  
20 hereby incorporated by reference herein) discloses a method by which a circuit board containing power conversion elements is coplanar located over a circuit board containing an integrated circuit. The interconnect between the power conversion substrate and the integrated circuit substrate utilizes pins which do not provide a low impedance power path to the integrated circuit. Further, the McMahon device cannot be easily disassembled  
25 because the pins are permanently connected to the substrates. As another example, U.S. Patent 5,619,339, (which is hereby incorporated by reference herein) issued to Mok discloses a printed circuit board (PCB) is vertically displaced over a multi-chip module (MCM) with electrical communication between the two substrates (the PCB and the MCM) established by a compliant interposer which contains "fuzz buttons" which communicate with pads located  
30 on each substrate. Although such an approach does provide for disassembly of the two substrates, e.g., the MCM and the PCB, the approach does not provide for large 'Z' axis



compliance to accommodate manufacturing tolerances, and does not teach the use of a contact design that is capable of handling large amounts of DC current. Further, this design requires the use of a compliant interposer. In order to handle such large amounts of current, the number of contacts would have to be increased dramatically, which would increase the inductance between the source and the load device. Furthermore, such a large array of such contacts would require a large amount of force to be applied to maintain contact and will not result in a space-efficient design.

From the foregoing, it can be seen that there is a need for a low impedance power interconnect between the power dissipating device and the power source. It can also be seen that this impedance must be low in inductance and resistance throughout a wide frequency band in order to ensure that the voltage drops across the interconnect are mitigated across it during dynamic switching of power. It can also be seen that the interconnect should provide large 'z' axis compliance and permit separation of the assembly without desoldering or similar measures.

#### SUMMARY OF THE INVENTION

To address the requirements described above, the present invention discloses an apparatus for providing power to a power dissipating device. The apparatus comprises a first circuit board and a second circuit board, and a plurality of compliant conductors disposed between first circuit board and the second circuit board.

The first circuit board includes a power conditioner circuit, and a first side and a second side having a plurality of first circuit board contacts thereon. The first circuit board contacts include a first set of first circuit board contacts communicatively coupled to a first power conditioner circuit connector and a second set of first circuit board contacts communicatively coupled to a second power conditioning circuit connector.

The second circuit board includes the power dissipating device mounted thereto and a plurality of second circuit board contacts disposed on a first side of the second circuit board facing the second side of the first circuit board. The second circuit board also includes a first set of second circuit board contacts communicatively coupled to a power dissipating device first connector and a second set of second circuit board contacts communicatively coupled to a second connector of the power dissipating device.

The plurality of z-axis compliant conductors includes a first set of z-axis compliant conductors disposed between the first set of first circuit board contacts and the first set of second circuit board contacts and a second set of z-axis compliant conductors disposed between the second set of first circuit board contacts and the second set of second circuit board contacts.

The first set of first circuit board contacts, the first set of z-axis compliant conductors, and the first set of second circuit board contacts define a plurality of first paths from the first circuit board to the second circuit board and wherein the second set of circuit board contacts, the second set of z-axis compliant conductors, and the second set of second circuit board contacts define a plurality of second paths from the first circuit board to the second circuit board.

The present invention provides a spring-like structure which disconnectably connects between two or more substrates (such as a printed circuit board or IC package) whereby the connection is disconnectable at least on one of the two sides. The interconnection system provides for an extremely low impedance through a broad range of frequencies and allows for large amounts of current to pass from one substrate to the next either statically or dynamically. The interconnection system may be located close to the die or may be further away depending upon the system requirements. The interconnection may also be used to take up mechanical tolerances between the two substrates while providing a low impedance interconnect. Due to the low impedance connection, the design permits the displacement of bypass capacitors on the circuit board having the power dissipating device, and placement of these capacitors on the circuit board having the power conditioning circuitry, resulting in ease of manufacturing and improved reliability of the power dissipating device assembly.

The present invention reduces or eliminates the need for supporting electronic components for the power dissipating device on the substrate, since the interconnect impedance between the power source and the electronic device is sufficiently low so that all or most of the supporting electronics can be located on the substrate containing the power source. Since the present invention does not use any socket connectors to supply power to the device, such socket connectors are freed to provide additional signals.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGs. 1A and 1B are diagrams showing exploded views of the interconnection system as placed between two substrates, e.g., a voltage regulator module (VRM) mounted over a power dissipating device;

FIGs. 1C-1E are diagrams showing different electrical arrangements of the contacts;

FIGs. 2A-2C are diagrams showing exploded views of the interconnection system as placed between a processor substrate and a motherboard, the interconnection system occurring on the sides of the processor substrate;

FIGs. 2D are diagrams depicting a view of section A-A of FIG. 2C;

FIGs. 3A-3C are diagrams showing a simple stackup cross-section of the interconnection system as placed between two substrates;

FIGs. 4A and 4B are diagrams showing an embodiment of a cantilever beam that may be used to implement the z-axis compliant contacts;

FIGs. 5A-5D are diagrams showing further embodiments of a cantilevered beam in which the different features of the beam construction are utilized to reduce the connection inductance of the compliant contacts;

FIG. 6A is an isometric view of an assembly showing multiple pairs of z-axis compliant conductors arranged in two rows within an insulating frame structure;

FIG. 6B is an isometric view of a pair of spring contacts in a scissor configuration;

FIG. 6C is a section view showing how spring contacts arranged in a scissor configuration can be used to interconnect the first and second circuit boards;

FIG. 6D is a plan view of the substrate in the embodiments illustrated in FIGs. 6A-6C;

FIG. 6E is a diagram illustrating another embodiment of the z-axis compliant conductors and contact pads on the first circuit board;

FIG. 6F is a diagram illustrating another embodiment of the invention in which a continuous linear contact pads on the second circuit board are used without opposing scissor configuration z-compliant conductors;

FIG. 6G illustrates an embodiment of the present invention wherein the z-axis compliant conductors are not permanently affixed to any contacts on either the first circuit board or the second circuit board, thus permitting easy disassembly;

FIG. 6H is a diagram presenting another embodiment of the present invention in which an x-axis compliant conductor interfaces with edge contacts on the second circuit board;

FIG. 6I is a diagram presenting another embodiment of the z-axis compliant  
5 conductors having reduced impedance;

FIG. 6J is a diagram presenting a cross section of the embodiment illustrated in FIG. 6I;

FIG. 7 is a plan view illustrating another embodiment of the present invention utilizing multiple rows of z-axis compliant conductors;

FIG. 8 is a diagram presenting a prior art stack up arrangement of a microprocessor  
10 substrate;

FIG. 9 is a diagram presenting an improved power distribution system made possible by the present invention; and

FIG. 10 is a diagram illustrating an embodiment of the present invention wherein the  
15 power conditioning unit is partitioned to provide multiple power signals, each differing in phase, and each being distributed to different sides of the power dissipating device.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following description, reference is made to the accompanying drawings which  
20 form a part hereof, and which is shown, by way of illustration, several embodiments of the present invention. It is understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

The present invention describes a low impedance interconnection system operably placed between the two substrates whereby the interconnect is either placed to one side of  
25 the device or devices or the interconnect system circumferentially surrounds these elements.

When a load change occurs in operation on one of these devices, a voltage will occur across the interconnect that can be described as shown below:

$$\Delta V = L \frac{\partial I_{Step}}{\partial t} + RI_{Step}$$

wherein  $\Delta V$  is the voltage across the interconnection system,  $L$  is the series loop inductance of the interconnect,  $R$  is the interconnect resistance, and  $I_{step}$  is the step-change in load current.

As shown above, the output voltage change  $\Delta V$  increases linearly with the loop inductance  $L$ . Further, where rapidly changing currents are involved (as is the case with step changes in current, it is critically important that the interconnect system provides for a low inductance between the two substrates. During such a current step, reducing the loop inductance  $L$  reduces the  $\Delta V$  that results from current changes, thus allowing power to be efficiently delivered from the current source to the load.

FIGS. 1A and 1B are diagrams illustrating a structure 10 which provides a power path from a power conditioning circuit to a high performance electronic power dissipating device via a plurality of paths, thus yielding very low impedance. The structure 10 comprises a main board assembly 14, an electronic assembly 13 having a high performance electronic power dissipating device, a power conversion assembly 12 and a heat dissipating assembly 11.

The electronic assembly 13 comprises a power dissipating device such as a microprocessor 134 assembled onto printed circuit board (PCB) or substrate 130 (hereinafter, the terms "printed circuit board", "circuit board" and "substrate" are used interchangeably). The circuit board 130 includes one or more circuit traces which deliver power to the die of the microprocessor 134. The circuit board 130 also includes circuit traces which route signals to a matrix of pins 131 communicatively coupled to microprocessor 134 I/O connectors. The microprocessor 134 is typically provided with a thermally conductive lid 133 in which the inside surface of the lid is in close thermal contact with the top of the die of the electronic device and the perimeter of the lid is sealed and attached to the surface of the substrate 130. Although the package described herein is provided with a lid the present invention does not preclude the use of unlidded package construction methods.

The signal pins 131 engage with a socket 141 which is mounted to a main board 140 both of which are a part of main board assembly 14. Signals from the main board assembly 14 are dispersed to other electronic devices to form a complete operating unit such as a computer. Other methods may be employed to route the signals from the substrate 130 to the main board 140 which may not utilize either pins or sockets.

The circuit board 130 includes a plurality of contacts 132. The contacts 132 can include power contacts and/or ground contacts. The power and ground contacts are communicatively coupled to power connectors or pads 135-137 of the power dissipating device 134, respectively.

5        FIGs. 1C-1E disclose several embodiments of the present invention showing different electrical arrangements of the contacts 132. In one embodiment, the power contacts include positive polarity power contacts 132A that are communicatively coupled to a positive polarity power connector or pad 135 on the power dissipating device 134 and negative polarity power contacts 132B that are communicatively coupled to a negative  
10        polarity power connector or pad 136 on the power dissipating device 134. The ground contacts 132C are communicatively coupled to a ground connector or pad 137 of the power dissipating device 134.

      In one embodiment of the present invention (illustrated in FIGs. 1D and 1E), the power contacts 132A and/or 132B are interleaved with the ground contacts 132C. In FIG.  
15        1D, each power contact 132A and/or 132B is adjacent a ground contact 132C, and each ground contact 132C is adjacent a power contact 132A and/or 132C. In another embodiment of the present invention, the positive polarity power contacts 132A are interleaved with negative polarity power contacts 132B in the same way. The foregoing interleaved or alternating design substantially reduces undesirable electrical impedance of the  
20        power path.

      In the embodiments shown in FIGs. 1A and B, the contacts 132 are disposed around the perimeter of the electronic device and are a part of the substrate structure 130.

      The substrate 130 generally comprises a number of conductive layers that are used to route both signals and power and ground. When routing power, layer pairs adjacent to each  
25        other form a very low electrical interconnect impedance between the power pads 132 and the die power and/or ground connectors (e.g. pads) of the electronic device 134. These layer pairs are connected to the power pads 132 in a closely coupled arrangement to the planes. A further description of the conductive layers and their arrangement with respect to the z-axis compliant conductors 124 is presented in conjunction with FIGs. 3A-3C below.

30        A power conversion assembly 12 is disposed directly above (along the z-axis) the electronic assembly 13. This assembly 12 comprises an interconnect substrate commonly referred to as a printed circuit board (PCB) 120, a power conversion circuit having

components 121 such as switching transistors, transformers, inductors, capacitors, and control electronics; output capacitors 123 and a compliant conductor assembly 122 having a plurality of z-axis compliant conductors 124. These power conversion components can be segmented according to the VRM circuit topology to optimize the impedance and power flow through the power conditioning circuitry. For example, in the case of a multiphase VRM, the topology of the VRM can be designed to provide one or more of the phases, each at the appropriate connector, thus minimizing the interconnect impedance and the required circuit board real estate. The plurality of z-axis compliant conductors 124 circumscribe and interface with the contacts 132 on the electronic assembly 13 to provide a conductive path between the power conversion assembly 12 and the electronic assembly 13 having very low inductance. Further, the conductor assembly 122 permits the power conversion assembly 12 and the electronic assembly 13 to be disassembled and separated without desoldering.

A significant advantage to injecting power to the power dissipating device in a circumferential manner is that the current in any portion of the power planes of the substrate used to deliver power to the power dissipating device can be reduced significantly. As an example, if four compliant contact assemblies are located on each of the four sides adjacent to the power dissipating device, then, the maximum plane current is one-quarter the total current of the device assuming that the current in the device has a uniform current density at its interface to the substrate. Furthermore, the path length is significantly lower than other methods to deliver power to the substrate further reducing the voltage drop in the power delivery planes of the substrate (see, for example, U.S. Patent No. 5,980,267, which is hereby incorporated by reference herein). Generally, the power delivery regulation budget is fixed and the power planes of the power dissipating device substrate are adjusted to maintain the desired budget either by increasing the number of planes or increasing the thickness of the planes as the current is increased or the budget is decreased. Circumscribed power delivery provides for significant reductions in both plane thickness and/or total number of planes.

In the illustrated embodiment, the conductors 124 of the conductor assembly 122 are attached (e.g. soldered or bonded) to the substrate 120. Further, the conductors 124 of the conductor assembly 122 are electrically coupled to the contacts 132 of substrate 130 through mechanical pressure applied to urge the substrate 120 towards the substrate 130.

Other variations of this structure are possible. As an example, the compliant conductor assembly 122 could be permanently attached to substrate 130 with contact pads on substrate 120 or, contact pads could be place on both substrates 120 and 130 and the compliant contact could provide pressure contacts to both substrates. Note that some of the interconnect compliant contacts may be used for control and sense interfaces between the power circuitry in assembly 12 and the electronic assembly 13. Finally, note that substrate 120 has an aperture to allow for the lid 133 to pass through and thermally couple to the heatsink assembly 11.

In the past, it has been necessary to position bypass capacitors on substrate 130 to provide for the transient current demands of the electronic device on the substrate. This has reduced the reliability of the electronic assembly 12 which is relatively much more expensive than the other assemblies. Thus, it is desirable to increase the reliability of this assembly to the highest degree possible. Because the interconnect inductance of the compliant contacts 122 is extremely low it is possible to position the necessary bypass capacitors 123 on the power conversion substrate 120. Further, note that these capacitors 123 are located directly above the conductor assembly 122 reducing the interconnect path length between the connector and the capacitors 123 (thus decreasing the impedance) to approximately the thickness of the substrate 120.

Heatsink assembly 11 is used to remove heat from both the electronic assembly 13 and the power conversion assembly 12. Heatsink assembly 11 comprises a finned structure 100, which is attached or is a part of base 111. Heat slug or mesa 112 is attached to or is a part of base 111 and is used to both disperse heat from the lid 122 and to mechanically conform to the proper vertical displacement between the lid of the microprocessor 134 and the heat sink base 111. Thermal interface materials may be used to thermally couple the lid 133 and the mesa 112 to the heatsink base 111 and the substrate 120/power components 121. The heatsink base 111 may also comprise cavities to accommodate any components on the top side of substrate 120 such as capacitors 123.

FIGS. 2A and 2B illustrate a structure 15 which is similar to structure 10 except the power conversion circuit components are located directly on the main board assembly 18. The structure comprises the main board assembly 18, a high performance electronic assembly 17 and a heat dissipating assembly 16.



Electronic assembly 17 is similar to electronic assembly 13 with substrate 170, lid 171 and pin matrix 172. However, contacts 173, which can be used as power pads, are located on the bottom side of substrate 170. In the illustrated embodiment, the contacts are disposed around the perimeter of the electronic device 172.

5 Main board assembly 18 comprises a main board 180 with power conversion components 181 making up a power conditioner circuit and compliant conductor assembly 182 having a plurality of z-axis compliant conductors 185 circumscribing a socket 183. As was the case with assembly 13, bypass capacitors 184 are placed on main board 180 directly under and in electrical communication with the z-axis compliant conductors 185. Heat sink assembly 16 is disposed above and is thermally coupled to the electronic assembly 17. The heat sink assembly 16, which removes heat from the electronic assembly 17, comprises a finned structure 160 and base 161.

10 Thermal interface material can be used between the base 161 and the lid 171 to thermally couple the base 161 and the lid 171. Thermal energy may also be removed from the power conversion components 181. This can be accomplished by providing a thermal conduction path from the bottom of the main board to an adjacent chassis surface. This can also be accomplished by simply providing sufficient airflow around these components so as to directly cool them. It is also noted that as was the case with the embodiments illustrated in FIGs. 1A and 1B, where ultimate electrical performance is not needed, compliant conductor assembly 182 and power components 181 may not need to circumscribe socket 183 and may be located on less than all four sides of socket 183.

15 FIG. 2C is a diagram of a structure 15 that is similar to that shown in FIG. 2A except that compliant conductor assembly 182 are at least partially enclosed and contained within the socket 186 which mounts to the main board 180. This facilitates the assembly of main board assembly 18.

20 FIG. 2D is a diagram presenting a section view (A-A) along one side of socket 186 showing the socket 186 and the compliant conductor 182. The socket 186 includes a section 186A that secures individual z-compliant conductors 182 in place by overmolding a base extension 187 of the conductors 182. Socket 186 includes a plurality female connectors 193 which accept pins that are communicatively coupled to the power dissipating device. Each female connector is also communicatively coupled to solder balls, which are reflow soldered to circuit pads 190 on main board 180. The power dissipating device is thus electrically

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connected to the main board 180, which, as shown in FIG. 2C, includes power components 181 for power conditioning.

The base 192 of compliant contact 182 is soldered to power contact pad 189. This is preferably accomplished during the same reflow solder step used to couple the solder balls 191 to the circuit pads 190 on the main board 180. Not shown are power connection paths to internal layers of main board 193 from surface contact 189.

FIGs. 3A-3C illustrate an embodiment of a stackup 30 configured to deliver power from a power conversion PCB 301 to a processor substrate 300. It will be recalled that a preferred embodiment of power delivery is to deliver power through alternating or interleaved contacts so as to reduce the interconnect impedance.

FIG. 3A is a diagram showing a plan view of the stackup 30 with the upper PCB 300 removed, showing the arrangement of adjacent z-axis compliant conductors 305 and 321 in the x-y plane. In one embodiment illustrated, the conductors are spaced approximately 50 mils apart, to decrease impedance. Further, the illustrated z-axis compliant (or, equivalently, compliant) conductors 305 and 321 are cantilevered beams having bases that are soldered or other wise affixed to contacts (or circuit pads) 303 and 320, respectively. The other end of the compliant contact is pressed against the contact (or circuit pad) of the upper circuit board 300.

FIG. 3B is a diagram illustrating a cross section (A-A) of one polarity of power delivery, e.g., the positive polarity, while FIG. 3C illustrates a cross section (B-B) of the negative polarity, the two sections adjacent to one another forming the preferred interleave pattern.

Referring to FIG. 3B, power conversion PCB 301 contains power layers 312 and 313 wherein layer 312 represents the negative power layer, and layer 313 represents the positive power layer the two of which are in close proximity to one another to effect a low impedance power interconnect. A plated through hole (PTH) 314 or similar conductor connects the positive power layer 313 to a surface pad 303. Z-axis compliant contact 305 is shown as a cantilever beam having a base that is soldered 304 to surface pad 303. The other end of the compliant contact 305 is pressed against circuit pad 302 on the surface of the substrate 300. A bypass capacitor 322 is located below the compliant contact 305 and on the side of the first circuit board 301 opposite contact 303. The bypass capacitor 322 includes first and second connectors such as conductive end metalization features 306 and

317, which are surface mounted and electrically coupled to pads 307 and 316, respectively on PCB 301. Circuit pad 307 is connected to layer 313 through an extension of PTH 314.

Circuit pad 316 is connected to layer 312 through an inter-connector such as the illustrated blind via 315. Preferably, the bypass capacitor 322 is disposed directly below the compliant  
5 contact and associated structure (e.g. displaced from the structure in substantially only the z-axis), as this offers lower inductance than embodiments where the bypass capacitor 322 is displaced laterally (in the x and/or y axes as well).

In the illustrated embodiment, layer 308 of substrate 300 is assigned a negative  
10 power polarity while layer 309 of substrate 300 is assigned a positive power polarity. Like layers 312 and 313, in the PCB 301, layers 308 and 309 are in close proximity to one another to achieve a low impedance power interconnect. A power dissipating device located on substrate 300 can therefore receive power through layers 308 and 309 of the substrate 300. Circuit pad 302 is electrically connected to layer 309 through one or more blind vias 310 thus  
15 forming a low impedance interconnect from layer 313 through PTH 314 to pad 303 then through compliant contact 305 to pad 310 and then through blind vias 310 to layer 309. Note that layers 308 and 309 are located on or near the surface of substrate 300. This frees the substrate 300 to use the other layers (represented as layers 311) for signal interconnect for the power dissipating device without topological complications that arise from designs in which the power and ground layers are disposed away from the bottom surface of the  
20 substrate.

Referring again to FIG. 3C, (which illustrates a cross section (B-B) of the negative polarity, thus forming the preferred interleave pattern with the cross section A-A in FIG. 3B) the negative polarity power interconnect is achieved by PTH 319 connecting layer 312 to  
25 surface contact (e.g. pad) 320 adjacent the positive polarity surface contact or pad 303 on the inner side of PCB 301. Compliant contact 321 is soldered 304 or otherwise coupled to surface pad 320 while the other end of the compliant contact 321 is pressed against (surface) layer 308 of substrate 300. Note that contact point for compliant contact 321 is shown as a point (or more specifically, a line segment along the y-axis) on layer 308 however, this contact area may be a unique area of layer 308 in which the surface is locally processed to  
30 provide special characteristics for this contact point such as gold plating over a nickel undercoat to improve the contact characteristics of the contact. Surface pad 310 may be processed in a similar manner.

Finally, capacitor 322 may be the same bypass capacitor as shown in FIG. 3B or an additional bypass capacitor connected to planes 312 and 313 through an extension of PTH 319 to surface pad 316 and blind via 318 to surface pad 307. The result of the above is to provide a very low compact and low inductance compliant connection between PCB 301 and substrate 300 with the two substrates being separable. Furthermore, because the interconnection method provides for a very low inductance connection it is possible to either eliminate or considerably reduce bypass capacitors on the substrate 300 containing the power dissipating device.

Because such substrates are constructed such that the interconnects between layers 308 and 309 are blind vias 310 which pass only between layer to layer and not through the entire substrate, signal layers 311 and additional power/ground layers (if any) will not be permeated with large numbers of via interconnects (such as 310) as would be if power entered from the top side of substrate 300. This has the benefit of freeing up signal routing space in these layers (such as 311) where the number of via interconnects are substantially reduced due to the entrance of power to the bottom side of substrate 300. The embodiment shown in FIGs. 3A-3C is superior to other interconnect designs wherein the capacitor is not placed below the z-axis compliant conductors and on the opposing side of the circuit board with the power conditioning circuitry. For example, if the capacitive element were placed on the second side of the first circuit board (the same side as the z-axis compliant conductor) and adjacent to the spring members, the length of the conductive path and hence the impedance of the interconnect would include not only the vias or PTHs traversing in the z-axis, but also traces or planes in the x-y plane. By placing the capacitive element 322 on the side of the circuit board opposing the z-axis compliant conductor and directly over (or under) the z-axis compliant conductor, the length of the conductive path (and hence the impedance) is substantially reduced. The conductive path length (and hence, the impedance) is further reduced by selecting the span of the capacitive element 322 and related structures (e.g. pads 307 and 316) to be substantially the same as the span (the length in the longitudinal, or x-axis, direction) of the z-axis compliant conductor. With the length of the conductive path minimized capacitive elements on the second circuit board (or substrate) can be removed, which improves manufacturability and reliability as well.

FIGs. 4A and 4B illustrate an isometric view of one embodiment of a U-shaped z-axis compliant conductor 40. The conductor 40 comprises a base 401 which can be soldered

or otherwise bonded to a substrate while contact surface 400 is pressed against a pad on an opposite substrate. FIG. 4A shows the conductor 40 in the uncompressed state while FIG. 4B shows the conductor in the compressed state. In the illustrated embodiment, the contact surface 400 is formed by an S-shaped portion having a curved surface. The curved surface assures that the conductor 40 presents a surface parallel to the circuit board above the contact 40.

FIGs. 5A and 5B illustrate an isometric view of another embodiment of the z-axis compliant conductor 50. The conductor has a base or first shaft portion 502 having a first end 504 and a second end 506 distal from the first end 504. The base 502 is generally soldered to a substrate contact. A U-shaped bend portion 508 is coupled to the first shaft portion 502. The U-shaped bend portion 508 includes a first end 510 adjacent and coupled to the first shaft portion second end 506 and a second end 512. A second shaft portion 514 is coupled to the U-shaped bend portion 508. The second shaft portion includes a first end 516 adjacent and coupled to the U-shaped portion second end 512. Second shaft portion is adjacent and coupled to a second U-shaped bend portion 520. The second U-shaped bend portion comprises a first end 522 adjacent and coupled to the second end 518 of the second shaft portion 514 and a second end 524. The second U-shaped bend portion is adjacent and coupled to a third shaft portion 526 disposed between the first shaft portion 502 and the second shaft portion 514. The third shaft portion 526 includes a first end 528 adjacent and coupled to the second end of the second U-shaped bend portion 520 and a second end 530 distal from the first end 528. Bend portion 532 is disposed at the second end 530.

The conductor contact surface 534 is pressed against a pad on an opposite substrate. The contact beam is then wrapped around and returns to the upper surface of base 502 forming a secondary contact 536 to the base 502. This embodiment has improved (reduced) connection inductance compared to the embodiment illustrated in FIGs. 4A and 4B because the mutual coupling between path 538 and path 540 is relatively low which establishes semi-independent and parallel connection paths between contact surface 534 and the base 502.

FIGs. 5C and 5D illustrate an isometric view of still another embodiment which is similar to that described in FIGs. 5A and 5B. FIG. 5C illustrates this embodiment in the uncompressed state whereas FIG. 5D illustrates the embodiment in the compressed state. This embodiment further comprises a third u-shaped bend portion 557 coupled to the distal

end 530 of the third shaft portion 526, a fourth shaft portion 555 coupled to the third u-shaped bend portion 557. The fourth shaft portion 555 includes a contact portion 556 distal from the third u-shaped bend portion 557. When compressed, the contact portion 556 establishes an additional third path between the contact point 552 and the base 502 that passes through the fourth shaft portion 555, the third u-shaped bend portion 557 and to the base 502. This embodiment has still further reduced inductance over the embodiment in FIGs. 5A and 5B because there are now three semi-independent paths 551, 553 and 555 between the contact surface 552 and the base 550.

Individual conductors can be grouped so as to ease assembly of the conductor onto a PCB or substrate using soldering or other joining processes. One method is to extend a surface feature (such as 401) of the conductor to an area outside of the active portion of the conductor which is joined to a common bar during the stamping and forming fabrication process and then to overmold this extended feature with an insulating plastic resin up to the common bar but not including the bar. The bar is then cut off leaving a set of individual isolated contacts that are mechanically joined and can be handled during assembly as one unit.

FIGs. 6A-6C illustrate another embodiment of the invention in which z-axis compliant conductors similar to those shown in FIGs. 5A and 5B are arranged in a scissor configuration.

FIGs. 6A and 6C illustrate an isometric view of the assembly 60 showing pairs of z-axis compliant conductors 600A, 600B, 600C, 600D (hereinafter alternatively referred to as first set or row of z-axis compliant conductors 600) and 601A, 601B, 601C, 601D (hereinafter alternatively referred to as second set or row of z-axis compliant conductors 601). Each of the conductors in each row 600, 601 of the assembly 60 comprises an interface portion 668 and 669 disposed away from the base of the conductor that is urged against the contact on the second circuit board. Further, each row 600, 601 of assembly 60 is preferably assigned a separate power polarity, e.g., row 601 might be assigned negative power polarity and row 600 might be assigned a positive power polarity. The conductors of the first row 600 and the second row 601 are thereby interleaved to form conductor pairs resulting in a low inductance power path.

Each of the conductors 600, 601 are held in place by an assembly such as overmold frame assembly 602 having an outer portion 602A and an inner portion 602B. In the

illustrated embodiment, the assembly holds the z-axis compliant conductors in place about at least a portion of the periphery of the power dissipating device. Hole 667 is an alignment feature that may be desirably placed in the molded assembly 60 to align the assembly 60 to the PCB (e.g. PCB 120) during soldering.

5           FIG. 6B illustrates an isometric view of a pair of spring contacts 600A, 601A in the scissor configuration. The base 612 of each contact in the row of contacts is extended to overmold 602 as described in the preceding paragraph to simplify assembly. In this arrangement, overmold outer portion 602A and overmold inner portion 602B are desirably joined at their respective ends to form the overmold assembly. An advantage of this  
10       configuration is that there is no resulting net torsional force about the y or z axes.

          FIG. 6C is a section view (section A-A illustrated in FIG. 6A) presenting an example where the scissor contacts described above are arranged in a stackup 61 to deliver power from a power conversion PCB 608 to a processor substrate 609. The circuit pads 610 on PCB 608 require isolation between adjacent pads in the y-direction, because they will have  
15       alternating positive and negative power polarities. However, of significant importance is that contacting pads 605 and 606 on the processor substrate 609 can be arranged to be a continuous linear pad in the y-direction. This provides for relaxed tolerances in the alignment of the processor substrate 609 to the power conversion substrate 608 or PCB, and reduces the net torsional force on the two substrates. Note that bypass capacitor 607 may be  
20       installed beneath the contact arrangement 61 in a manner similar to that as described in FIG. 3.

          One technique of reducing the effective inductance of a multi-conductor connector is to assign adjacent conductors opposing current polarities. The magnetic fields of the opposing currents partially cancel each other, thus reducing the effective inductance of the  
25       overall connection. However, the effectiveness of this configuration is strongly dependent upon the configuration of the multiple conductors. In a simple configuration wherein the opposing faces of adjacent conductors are relatively narrow compared to their separation, the magnetic coupling between the conductors does not provide a substantial amount of magnetic field cancellation. However, if the separation distance between the substrates in a  
30       parallel plane connection scheme such as illustrated in FIG. 6C is small relative to the width of the conductors, then the magnetic field coupling between the planes becomes more significant, thus resulting in a lower inductance. This effect can be enhanced by arranging

the conductors in each row 600, 601 of the connector in an opposing configuration as shown in FIG. 6B. Then, the current from one pair of conductors (e.g. 600A and 601A) now flows across each end of the connector bases and in internal planes of the substrates 608 and 609. This current magnetically couples with the current flowing in the non-base portions of the scissored conductors (600A and 601A), reducing the overall inductance of the connection between substrates 609 and 608. For the effective inductance of this scissored arrangement to be less than the effective inductance of a non-scissored arrangement, the angle that the conductors make with the PCB/substrate plane must be less than a particular value  $\theta = f(t, w, s)$  wherein  $t$  is the conductor thickness (here, assumed uniform),  $w$  is the width (also assumed uniform) and  $s$  is the separation between adjacent conductors.

FIG. 6D is a plan view of substrate 609 further illustrating the concept of the continuous pads 605 and 606 that surround power dissipating device 613. In the illustrated embodiment, the pads 605 and 606 are formed into a continuous rings, one inside the other.

FIG. 6E illustrates a variation on the scissor contact design described in FIGs. 6A-6C. A base portion 670 of an elongated z-axis compliant conductor 630 (of a scissor pair) is soldered to pad 632 on PCB 608. The upper cantilevered beam portion 634 of compliant conductor 630 is pressed against contact pad 631 of substrate 609 as previously described. However, in this configuration, rather than the secondary contact wrapping around and returning to the top surface of the base 502, the contact 630 wraps around portion 635 of compliant conductor 630 returning to a separate contact pad 633 on PCB 608. Although both contact pads 632 and 633 are in electrical communication with the same power conditioning circuit, (e.g. through vias and conductive layers in the substrate 609) the advantage of this configuration is that the mating surfaces 636 of contact pad 633 and contact portion 635 are not involved in the soldering process and as a consequence there is no risk that solder used to couple the base 670 of the conductor 630 to the pad 632 may flow into the contact region of the secondary contact 633. Additionally, because the secondary contact is further removed from the initial contact path there is less mutual coupling between the two contact paths which results in a lower overall connection inductance.

FIG. 6F illustrates another embodiment of the present invention. In this embodiment, the stackup configuration 64 includes a first and second set of U-shaped z-axis



compliant conductors (640 and 641, respectively) that are displaced from one another along the x-axis. The x-axis displacement allows contact pads 644 and 645 to be constructed in a continuous linear fashion on substrate 609 similar to the embodiment shown in FIGS. 6A, 6B and 6C, without requiring that the first and second set of conductors 640, 641 be oriented 180 degrees from each other. Z-axis compliant conductor 640 is soldered or otherwise connected to contact pad 642 on PCB 608 which is connected to one polarity of a power circuit (e.g., as shown in FIGS. 3A-3C) while z-axis compliant conductor 641 forward of conductor 640 and displaced from conductor 640 in the x-axis is also soldered or otherwise electrically coupled to contact pad 643 of a second polarity of a power circuit (also as shown in FIGS. 3A-3C).

The embodiments illustrated in FIGS. 6A-6F have numerous advantages. First, as described above, they permit substantial misalignment between the z-axis compliant conductors and the contacts on the opposing circuit boards in the direction of the adjacent conductors (e.g. in the y-axis direction in FIGS. 6B-F). Second, a nearly contiguous line of vias disposed through the pad region can be used for connecting the contacts to conductive planes within the circuit board, thus allowing a lower interconnect impedance in the substrate 609. Third, as described further below with respect to FIGS. 6I and 6J, the arrangement shown in FIGS. 6A-6C allows for improved electromagnetic coupling between each spring over arrangements where each of the z-axis compliant conductors are arranged in a single row.

FIG. 6G illustrates a stackup configuration 65 in which the z-axis compliant conductor is removably attached (e.g. not soldered, bonded, or otherwise permanently attached) to either substrate 609 or PCB 608. In this configuration insulating (plastic, for example) overmold element 652 retains compliant conductor 651. Additional conductors (disposed in the y direction) are also retained by plastic element 652, forming a contact assembly that can be installed at the time of assembly of substrate 609 and PCB 608. As before, section 653 of compliant conductor 651 is pressed against contact pad 605 on substrate 609 and section 654 is pressed against contact pad 655 of PCB 608 completing one half of a power circuit between PCB 608 and substrate 609. The other half of the power circuit is completed by the adjacent conductor (displaced from conductor 651 in the y-axis). It is also recognized that an arrangement such as that which is shown in FIGS. 6F and 6G

may also be applied in a similar manner as to the arrangement in FIG. 6C, with opposing or staggered conductors, using a multiple-part or shaped overmold.

FIG. 6H illustrates still another arrangement wherein a compliant conductor may be used to provide power to a power dissipating device. In this arrangement, the plurality of first circuit board contacts 664 are disposed on the edge of the first circuit board. While only a single contact 664 is shown, a plurality of contacts, electrically isolated from one another and distributed in the y-axis, are disposed on the edge of the first circuit board 609. Section 661 of each of the x-axis compliant conductors 660 is urged against an adjacent side contact 664 which is electrically connected to internal conductive plane 662 of substrate 664. The internal conductive plane 662 is electrically coupled to the power dissipating device (via conductive planes, vias, and the like) to feed power to a power dissipating device disposed on the substrate 664. The other end of conductor 660 is soldered or otherwise electrically connected to contact pad 665 of PCB 608. Electrical connection between the contact pad 665 and to power layers of the PCB 608 can be made by a combination of plated through holes, vias and interconnecting conductive layers in the PCB 608.

Only one contact is shown in the section view of FIG. 6H. However, it will be understood that a multiplicity of compliant contacts 660 can be arranged along the y-axis and the multiple compliant contacts 660 can interface with a corresponding multiple of edge contacts 664, each electrically isolated from the others, to form multiple power connections between PCB 608 and substrate 664, wherein alternating contacts 664 connect to alternate polarity power plane 663. In a preferred embodiment, the contacts 660 and related structures circumscribe all sides of substrate 664 to form a very low impedance power interconnect path between PCB 608 and substrate 664. The conductor 660 can also be designed with a bend to restrain the first circuit board 609 in place, if desired.

FIG 6I illustrates one embodiment of the z-axis compliant conductor design. The illustrated z-axis compliant conductor pair which form a part of a larger array of conductors. Conductor 671 carries current in of one polarity while adjacent conductor 672 carries current in an opposite polarity. As before, a practical method of assembling such an array is to join the individual conductors with an overmolded plastic resin 673 that supports the conductors 671 and 672. Of note is that each of the conductors 671 and 672 are provided with a slit 677 and 680 which creates two separate current paths in conductors 671 and 672 over a substantial portion of the length of the conductors. These separate current paths are

identified as 675, 676 for conductor 671 and 678 and 679 for conductor 672. The result of this arrangement is to reduce the overall connection inductance between a PCB and a substrate.

The reduced connection inductance of FIG. 6I can be explained by referring to FIG. 6J which illustrates a section view through the conductor sections as indicated by A-A. The top portion of FIG. 6J illustrates the arrangement where there is no slit, forming conductors 681 and 682, whereas the bottom portion illustrates the arrangement where the slits 677 and 680 form conductors 685, 686, 687 and 688. The inductance of each conductor, 681 or 682, in the configuration without the slit is:

$$L_{681,682} = 2 \cdot \ln \frac{S1}{0.2235 \cdot (t + W1)}$$

For the configuration with the slit 677, 680, the inductance of the pair of conductors 685 and 686 or 687 and 688 can be determined by calculating the inductance of each conductor and then noting that the conductor pair are in parallel with one another. The general equation for the inductance of a multi-conductor configuration where the current in all conductors is equal (this is the case since, by symmetry, a continuous set of paired contacts as shown in FIG. 6I must have the same current in each path) is:

$$l = 2 \cdot \ln \frac{GMD}{GMR} 10^{-7}$$

where *GMD* is the geometric mean distance from the first group of conductors to the second group of conductors and *GMR* designates the geometric mean of the individual geometric mean radii of the group together with the wire-to-wire distances among the conductors of that group. Applying the forgoing relationships yields an expression for the inductance of the conductors 685, 688, 686, 687 is as follows:

$$L_{685,688} = 2 \cdot \ln \frac{\sqrt{(S2 + S3)(S2 + 2 \cdot S3)}}{\sqrt{.2235 \cdot (t + W2) \cdot S3}} 10^{-7}$$

$$L_{686,687} = 2 \cdot \ln \frac{\sqrt{S2 \cdot (S2 + S3)}}{\sqrt{.2235 \cdot (t + W2) \cdot S3}} 10^{-7}$$

The pair inductance then is simply  $L_{685,688}$  in parallel with  $L_{686,687}$ :

5

$$L_{pair} = \frac{L_{685,688} \cdot L_{686,687}}{L_{685,688} + L_{686,687}}$$

When the above equations are applied to practical conductor geometries, substantial reductions in inductance can be achieved by providing a slot in the contact arrangement as shown in FIG. 6I.

10 It is understood that in all of the previously described conductor embodiments, it is important to design the contact arrangement such as to avoid rotational forces that may be imparted to the base of the contact wherein the base is soldered to one of the substrates. The reason for this is to eliminate normal forces that are not in compression (along the z-axis) which apply a torsional force to the base portion of the conductor, and which may  
15 result in solder creepage, and ultimately the failure of the solder joint between the base of the conductor and the substrate pad. This can be accomplished by designing the conductor so that the interface portion that contacts the second circuit board contact and the base portion that contacts the first circuit board contacts are disposed substantially only along the z-axis from one another (e.g. either above or below each other, but not displaced in the x-y plane).  
20 This can be achieved, for example as demonstrated in the foregoing description where the compliant conductor beam is folded over the base of the conductor.

It is also desirable to design the conductor and contacts to cooperatively interact with each other to minimize contact resistance and insure good electrical connection. This can be accomplished, for example, with the S-shaped conductor portions (such as that which  
25 is illustrated in FIGs. 4A and 4B, or other electrical contact-enhancing designs).

FIG. 7 is a diagram illustrating a plan view (looking up into PCB 120) of another embodiment of the present invention. As in previous embodiments, the z-axis compliant conductors, as well as the contacts on the PCB and substrate that interface with the z-axis compliant conductors are disposed about the periphery of the power dissipating device.

Further, the power and ground (or positive and negative power) conductive paths formed by the conductors and contacts were interleaved to reduce inductance. In the embodiment illustrated in FIG. 7, the set contacts on the first circuit board and the set of contacts on the second circuit board are separated into two subsets of contacts, and the z-axis compliant  
5 conductors are separated into two subsets of conductors as well. As was the case in the embodiments discussed previously, the first subsets of the contacts on the first and second circuit boards and the z-axis compliant conductors are disposed circumferentially around the power dissipating device. However, in this embodiment, the second set of contacts on the first and second circuit boards and the z-axis compliant conductors are disposed  
10 circumferentially around the first subset of contacts on the first and second circuit boards and the z-axis compliant conductors. The result is two "rings" of circuit paths from the first circuit board, through the first subset 122A and the second subset 122B of z-axis compliant conductors, to the second circuit board, wherein each ring includes a plurality of interleaved ground and power paths. The multiple "rings" of contacts 122A and 122B, one behind and  
15 disposed circumferentially about the other, are used to achieve even lower interconnect impedance between the PCB 120 and the substrate 130. This is accomplished at least in part because each of the multiple rows of contacts 122A and 122B effectively couple in parallel.

One of the advantages of the present invention is that it permits simplification of the power/ground/signal interconnect between related printed circuit boards. FIG. 8 is a  
20 diagram illustrating a typical stackup arrangement 5 having power/ground/signal interconnect contention problems. The substrate 847 of the stackup 5 includes conductive circuit layers 831, 834, 836, 839, and 841, and insulating layers (832, 835, 837, 840, and 842) reside between the circuit layers 831, 834, 836, 839, and 841. A surface layer 826 typically is used for making contact through bumps to power dissipating device 827. The number of  
25 insulating and conducting layers may be increased or decreased depending upon the signal and power demands of the power dissipating device.

In most integrated circuit packages, power enters from pins 845 disposed on the opposite side of the power dissipating device 827 and is distributed through power vias 833, 838 in the substrate 847. The power dissipating device 827 has connectors for power and  
30 ground (828, 829 shown) which connect to a surface layer 826 of substrate 847. To ensure a low impedance DC power distribution path, multiple power vias 838 and ground vias 833 must pass through substrate 847 to connect with multiple power and ground pins (e.g. 844

and 843 respectively). Power and ground is distributed from contacts 845 including lower contacts 844 and 843 (which may be a large numbers of pin connections in a socket).

Power contacts 844 are coupled to one or more power planes 841 and 836 by one or more power vias 838, 848, and thence to power bumps 829. Similarly, ground contacts 843 are coupled to one or more ground planes 839, 834 by one or more ground vias 849 and thence to ground bumps 828. Signal contacts, e.g., 830, connect to conductive signal layers 831 and then typically distribute signals to the periphery of the device through signal vias, e.g., 825, and then down into a signal contact, e.g., 846, for distribution to other components communicatively coupled to the contact 846 (for example, a motherboard).

FIG. 9 is a diagram of an improved power distribution system configuration 90 in which power taps 901 are provided through the top side of substrate 923 instead of through the bottom. Power taps 901 represent where the compliant conductors make contact to the pads on the top surface of the substrate to distribute power from a power source to the power dissipating device 906 on substrate 923. Power dissipating device 906 on substrate 923 is connected as described in FIG. 8, except that that power layer 908 does not require substantial via distributions to lower layers such as layers 912 and 914. Power enters power taps 901 whereby the power layer 902 connects to the right power tap 901B and the ground plane 910 connects to left power tap 901A through via 903. Ground plane 910 then connects to vias 924, which in turn connect to ground bumps 905 on power dissipating device 906. Additionally, power is routed from power plane 902 to power bumps 904 on power dissipating device 906. This completes the power distribution path for the substrate stackup 923 from the source to the load, e.g., the power dissipating device 906. Note that for illustrative purposes, the bumps 904, 905 on power dissipating device 906 are raised slightly off of the power plane 902.

Signal connections from power dissipating device 906 may now be routed to one or more bumps 907, which connect to one or more vias 915 which route to one or more signal planes 917. Other signals may now be distributed to pin connections (or alternatively other bump interconnects such as in an interposer to substrate connection) for connection to pins (such as 921 through vias similar to 922) which connect to a socket-like interconnect or PCB. Ground connections 920 through vias 919 and ground plane 914 may now be used for signal reference only rather than for power distribution as well. As in FIG. 8, insulation layers 909, 911, 913, 916, and 918 make up the rest of the substrate 923 construction.

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This embodiment allows for a reduction in the number of layers because that power distribution is facilitated predominately through the top two layers 908, 910 of substrate 923. Additionally, since the power and ground conductive layers are disposed on a power dissipating device side of substantially all of the conductive signal layers, the passage of power through the planes of the conductive signal layers is minimized. The distribution of signals the x-y planes is also improved. This is due to elimination or reduction of the number of vias for power and ground distribution in substrate 923 that would normally have been used to connect to pins 845 as described in FIG. 8. Through elimination of the power and ground vias in these lower layers (utilizing the top two layers), x-y plane real estate is henceforth available for additional signal routing in the lower layer(s), e.g., 917.

FIG. 10 illustrates an embodiment of the present invention wherein the power conditioning circuit or module 1000 includes a plurality of power conditioning submodules 1001A-1001D, which together provide a power signal having a plurality of phases. In this embodiment, the topology of the power conditioning circuit 1000 delivers power to a plurality of compliant conductors 1003 advantageously arranged to apply different phases of the power signal to different sides of the power dissipation device 1006. The power dissipation device 1006 is shown connected to power and ground planes 1005 and 1004 located on substrate 1002. It is understood that the power dissipation device/substrate 1006/1002 resides at a level either above or below the voltage regulation module 1000. Power and ground planes 1005 and 1004 then connect to VRM 1000 through compliant conductors 1003 which circumscribe power dissipating device 1006 wherein the ground of each phase connects to ground plane 1004 and the voltage out of each phase connects to the power plane 1005.

Topologically, each phase is represented by an input voltage ( $V_{IN}$ ) to two FET switches and an L-C output circuit. In the illustrated embodiment, each phase operates 90 degrees out of phase with the other adjacent to it. Because of the organization of the phases and due to the placement of the compliant conductors 1003 one may lay out the PCB of VRM 1000 in this topological fashion which improves routing and interconnect impedance due to the partitioning of each phase about the periphery of the power dissipating device. This allows the inductors, capacitors, and electronic drive circuitry (FETs, etc.) of each phase to be logically placed adjacent to a linear compliant conductor 1003 resulting in a superior layout and interconnect scheme which is synergistic with the topology of the VRM itself.

While the foregoing embodiment is described with respect to a four phase power signal applied to each of a four-sided power dissipating device, the principles described above can be applied to embodiments with fewer or more than four sides and power signal phases, or to embodiments with non-polygonal configurations (e.g. circular, for example).

In summary, the foregoing discussion discloses a low impedance power interconnect between the power dissipating device and the power source. The impedance of the power interconnect is low in inductance and resistance throughout a wide frequency band in order to ensure that the voltage drops across the interconnect are mitigated across it during dynamic switching of power. It can also be seen that the interconnect should provide large 'z' axis compliance. The arrangement also reduces or eliminates the need for supporting electronic components on the device substrate because the interconnect impedance between the power conditioning circuit and the device can be reduced to the point where all or most of the support electronics can be located on the substrate having the power conditioning circuit itself.

The present invention also significantly reduces contentious routing of power to the power dissipating device because the power interconnect impedance is significantly lowered and can be routed to one or more sides of the power dissipating device.

Further, since the upper layers of the power dissipating device substrate are used primarily for power distribution, the area on additional layers beneath the upper layers are free for use with for signal and other conductive interconnects. These other conductive interconnects can connect other interconnects or substrates beneath or above the stackup.

#### Conclusion

The foregoing description of the preferred embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. For example, the substrate contacts and compliant conductors can be disposed proximate the outer periphery of the substrates rather than proximate the power dissipating device as described herein. Further, the compliant conductors may be rigid instead of compliant, while still permitting the detachable design described herein. Also, the compliant conductors can be integrated with other assemblies



such as a socket, which might be used to interconnect signals to the microprocessor. Further, more than one linear set of contacts can be arranged to circumscribe the power dissipating device in a manner to increase the total number of contacts providing power and/or ground to the device, thus reducing the overall connection inductance and increasing total current carrying capability. The z-axis compliant contacts can also be configured so as to permit acceptance of stackup height variations.

It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto. The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

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